NMOS Pass Gates w/ a Dual-VDD Scheme Minimize Delay and Energy in a FPGA Interconnect in Sub-Threshold

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**ABSTRACT**

In this paper, we explore three different FPGA switchbox topologies – Tri-state Inverters (TSIs), Transmission Gates (TXs) and Pass Gates (PGs) – in search of finding the optimal choice for Sub-VT operation. By comparing the energy drawn by and the propagation delay through each of the structures in 90 nm technology, we conclude that using NMOS PGs in a Dual-VDD scheme (using a separate VDD for the Gates of the PGs) gives the best tradeoff between performance and energy consumption. After verifying this claim through simulation, we attempted to create a mathematical model with which we could use Elmore Delay calculations to determine which topology would be optimal for the interconnect. However, we found that the Avg. Resistance method does not adequately illustrate the “Effective Resistance” of the structures as the signal propagates, and therefore an RC approximation would be entirely too inaccurate.

# INTRODUCTION

Field Programmable Gate Arrays (FPGAs) are re-configurable circuits. A typical look up table-based FPGA architecture consists of configuration logic blocks (CLB) which contain a cluster of basic logic elements (BLE), each of which contains 4 input (16:1) Look Up Tables, a Multiplexer and flip-flops (FF). FPGAs also contain a programmable mesh of interconnect, which consists of wires, connection boxes (which connect CLB’s to interconnect), and Switch Boxes (which connect routing channels for inter-CLB routing). FPGAs are attractive because, due to its reconfigurability, they bridge a gap between flexibility and efficiency. The most efficient hardware are ASICs (Application Specific Integrated Circuits) but they lack flexibility as they perform pre-defined functions. GPPs (General purpose processors) exhibit great flexibility but poor energy efficiency. FPGAs display greater energy efficiency than GPPs, while being more flexible than ASICs in that they can be reconfigured for different applications. A major issue preventing ubiquitous implementation of FPGA technology is the large interconnect. FPGA Interconnect has about 25X to 50X the parasitic capacitance of an inverter, dissipates 60-70% of the total power in an FPGA, and consumes roughly 75% of the FPGA area. Issues with Sub-VT implementation, such as variability and leakage, exacerbate these issues. Clearly, optimizing the FPGA Interconnect for higher performance and lower energy consumption during Sub-VT operation provides many interesting challenges. There are multiple areas where we can optimize the interconnect design, such as wiring, connection boxes and switch boxes. In this paper we focus on switch box topology.

Section 2 describes our design choices for the test circuits we used to simulate the FPGA Interconnect. In Section 3, we discuss how TSIs, TXs, and PGs compare to each other w/o increasing the gate voltages of the structures. In Section 4, we will show what effect boosting the gate voltage has on each structure, and then compare them again. In Section 5, we discuss our attempt at creating a mathematical model for the FPGA interconnect.

# TEST CIRCUITS

To test the FPGA Interconnect efficiently, we elected to use a simplified model of a worst case FPGA interconnect. Our goal was to isolate the switchboxes themselves by idealizing the other parts of the interconnect (Connection Boxes, wiring, etc.) and focusing entirely on the switches. Our test circuit consisted of a buffered input square wave signal, which propagates through 10 switches before terminating at an inverter.

We chose a 10-switch interconnect circuit design because we hypothesize that would be a worst-case scenario. For an FPGA signal to travel through 10 switches, that would require the signal to have to jump to 10 different wires throughout the interconnect, an occurrence that is unlikely [3].

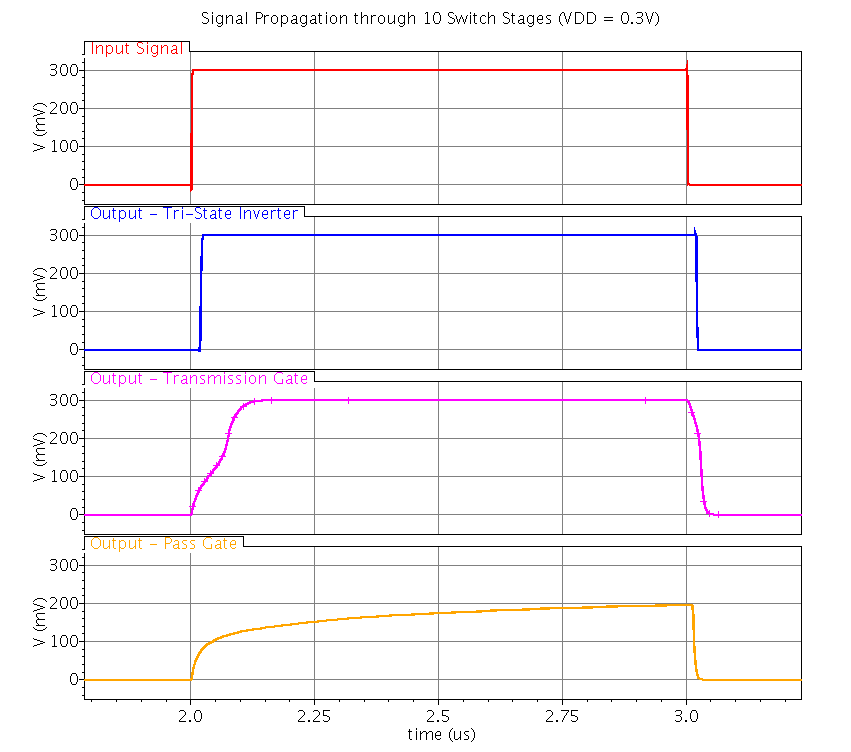
The two main metrics we measured were delay and energy drawn from the supply. We took delay measurements through the entire network (between the input and the output of the 10th switch). We used 50% of the rise or fall of the signal as our reference for calculating the delay, and we averaged the High-to-Low (H-L) and the Low-to-High (L-H) to obtain the propagation delay. We observed the current draw from VDD of the entire circuit, and calculated the energy over one signal period, using that current, VDD, and the signal period (E=PT = VIT).

# SINGLE VDD SCHEME RESULTS The three topologies (TSIs, TXs, and PGs) were compared on both performance (delay) and energy consumption. We then looked at Energy-Delay (ED) curves to make an overall claim about the different structures while keeping both performance and efficiency in mind.

## Performance Comparison

In looking at the signal propagation through each of the structures at 0.3 V (Figure 1), it’s clear to see that TSIs have by far the best performance. The transitions are very sharp compared to the other two structures, which minimizes static current in the receiving inverter. It is also clear to see that the PG is less than ideal for the current circuit, mainly because the signal comes nowhere near full swing on the low-to-high transition of the signal, peaking at only about 180mV of the 300mV total swing. This phenomenon occurs because when the signal is transitioning low to high, the source of the PG is rising, lowering VGS, which lowers the current through the transistor exponentially throughout the transition.

This provides a problem for two reasons: long propagation delay and increased static current. We measured delay between the 50% points of the input and the output transitions, so a slow rising edge for the PG greatly increases the overall delay.

  
**Figure 1. Voltage Signal after 10 switches**

Additionally, because the transition takes so long, the signal spends more time between the digital values of 0 and 1 (0 and 0.3V respectively), and as a result both of the transistors in the receiving inverter are on for a longer period of time, which results in increased static current draw through that low impedance path to ground.

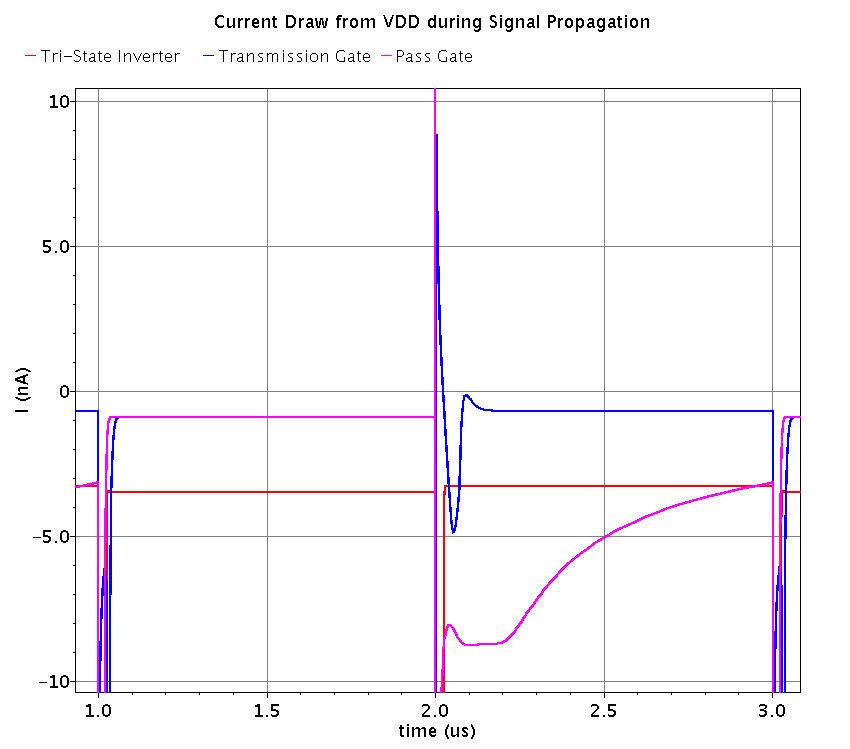
## Current Draw Comparison

In looking at the plot which shows the current drawn (Figure 2), TXs clearly have the advantage over the other two structures. The graph shows the expected peaks in current when the input switches L-H or vise versa (at times 1, 2, and 3 us). The more interesting phenomena happen during the low and high phases of the signal. Here, the current draw that is observed is due to leakage (through the switches, the buffer, and the receiving inverter) and due to static current in the receiving inverter. During the low phase, we see that the plots are mainly flat, with the PGs and the TXs showing negligible current draw compared to that of the TSIs. Each TSI is connected to VDD and leaks, which is why TSIs draw a larger constant current during the low phase of the input.

During the high phase of the signal, the impact of the PGs low swing is evident. Early in the transition, the current draw is much higher (nearly 3x) than that of the 10 leaking TSIs. Even at the end of the transition, the signal is at such a level that both of the transistors in the receiving inverter are “on,” which results in higher static current.

## E-D Curve Comparison

One way to make meaningful comparisons between different independent variables (knobs) in a circuit design is to look at ED Curves. These plots provide a way to look at the data and immediately make judgments concerning how well a design is suited for low energy or high performance applications. In looking at these three switch topologies, the ED curve (Figure 3) and the corresponding table (Table 1) both suggest the same conclusion we came to in looking at each facet individually: TXs as switches minimize energy consumption, and thus would be good for low power applications, whereas TSIs greatly minimize

 **Figure 2. Current Drawn from VDD by   
each Interconnect Model**

delay, so that if performance was the main metric, TSIs would be the ideal choice. PGs are by far the least ideal of the three options, with a delay that is on average 3.3x slower than PGs and an energy consumption that is on average 2x higher than TXs.

  
**Figure 3. Energy-Delay Curves for each Switch Box Model**

# DUAL VDD SCHEME

All of the issues with the PGs and their high energy consumption and their high delay characteristics stem from the fact that they “turn themselves off” – VGS lowers during the L-H transition, and the current through the PGs depends exponentially on VGS in Sub-VT. If PGs could pull signals high well, then they would ideally be similar to TXs, only with half of the area. The way we explored alleviating the L-H transition problem was by implementing a Dual-VDD design where the gate voltage, instead of being set to the same VDD as the signal swing and the drivers, is set to a different, higher VDD, which we will call VDDc [3]. This

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Delay (ns)** | | | | | |
| VDD (V) | 0.2 | 0.3 | 0.4 | | 0.5 |
| Tri-State | 132.1 | 20.3 | 4.5 | | 1.7 |
| Transmission Gate | 255.2 | 45.6 | 10.6 | | 3.8 |
| Pass Gate | 356.2 | 126.3 | 45.9 | | 17.3 |
| **Energy (fJ)** | | | | | |
| Tri-State | 1.2 | 2.5 | 4.4 | 7.2 | |
| Transmission Gate | 0.7 | 1.7 | 2.9 | 4.7 | |
| Pass Gate | 0.7 | 2.3 | 6.4 | 16.3 | |

**Table 1. Delay and Energy of simulated   
Interconnects of TSIs, TXs, and PGs**

increases VGS during the transitions, allowing for more current to travel through the PGs, lowering delay. The L-H transition is also faster now, so there is less static current flowing through the receiving inverter, lowering energy. These decreases in delay and energy consumption are essentially free in, because increasing the gate voltage doesn’t increase the current draw from VDD, since gate current in NMOS technology is negligible.

To implement the planned Dual-VDD scheme, we need to first find the optimal VDDc. Once we find the optimal VDDc, we need to then look at signal propagation, current draw, and the ED Curves again, to see how PGs fare among the other topologies in a now-Dual-VDD implementation.

## Finding Optimal VDD

While we believe we can increase VDDc and mitigate the PGs inability to pull high, it is clear that one cannot just increase VDDc indefinitely. Increasing the gate voltage too far will cause the gate current to no longer be negligible in comparison to the current through the devices, especially since the design is being optimized for Sub-VT implementation [2]. Table 2 shows how the delay and energy for the three structures change with an increased VDDc. PGs and TXs benefited in both delay and energy from an increased VDDc, whereas TSIs exhibited an increase in the energy drawn from VDD. Because each TSI is connected to VDD and draws from VDD, increasing VDDc increases the amount of current drawn from VDD, resulting in more energy drawn.

For all three topologies, a VDDc was 1 V above VDD (in this test case, 1.3V) optimized delay through the interconnect. For PGs and TXs, the same VDDc optimized energy. Boosting VDDc had the largest effect on PGs, which had over 96% reduction in delay and nearly 80% less energy with the higher VDDc. However, it’s important to note that TXs also showed higher performance and efficiency with a larger VDDc.

## Performance and Delay Revisited

Figure 4 shows the E-D curves for the three switch types again, only this time VDDc is boosted to 1V above VDD. Now, PGs clearly show lower energy and delay over the Sub-Vt range. Table 3 shows the new delay and energy numbers with boosted VDDc. On average, the PG network exhibits 2.2x less energy drawn and 1.6x less delay than the TXs. They display 7.5x less energy and 2.4x less delay than TSIs.

|  |  |
| --- | --- |
| **Delay Savings**  (VDD = 0.3 V, VDDc = 1.3 V) | |
| Tri-State | 42.8% |
| Transmission Gate | 86.2% |
| Pass Gate | 96.2% |
| **Energy Savings**  (VDD = 0.3 V, VDDc = 1.3 V) | |
| Tri-State | -0.1% |
| Transmission Gate | 75.7% |
| Pass Gate | 78.5% |

**Table 2. Delay and Energy Savings with a   
VDDc boosted by 1V**



**Figure 6. Energy-Delay Curves for each Switch Box Model   
(w/ optimized VDDc)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Delay (ns)** | | | | | |
| **VDD (V)** | **0.2** | **0.3** | **0.4** | | **0.5** |
| Tri-State | 78.1 | 11.6 | 2.7 | | 1.1 |
| Transmission Gate | 51.2 | 8.0 | 1.8 | | 0.8 |
| Pass Gate | 30.4 | 4.8 | 1.1 | | 0.5 |
| **Energy (fJ)** | | | | | |
| Tri-State | 1.4 | 3.0 | 5.3 | 8.6 | |
| Transmission Gate | 0.3 | 1.0 | 2.1 | 3.7 | |
| Pass Gate | 0.09 | 0.5 | 1.2 | 2.2 | |

**Table 3. Delay and Energy of Simulated Interconnects of TSIs, TXs, and PGs with boosted VDDc**

# RESISTANCE MODEL

Along with exploring different switch box topologies through circuit simulations, we want to create a model that adequately represents delay and energy. In doing so, we could determine which switch box topology is ideal without having to rely on simulations, which makes the determination process much more time efficient.

Our plan was to use an RC model for each structure, which will require an Average Resistance approach to calculating delay. Using an RC model allows easy expansion of delay calculations for one switch to networks of multiple switches by assuming Elmore delay. Thus, we calculated the thing using the Average Resistance Method [2]. The Average Resistance Method originally calls for using voltages and currents at the endpoints of the H-L and L-H signal transitions, but that will not work for our FPGA Interconnect model, because transistors do not behave like true resistors (see Figure 5). Because of the resistance profile of an NMOS or a PMOS transistor, using the endpoints would underestimate the NMOS resistance and overestimate the PMOS resistance. So instead, we simulate the resistance.

  
**Figure 7. Pass Gate Current vs. Voltage (VDS)**

To simulate the resistance, we used the voltage across an NMOS transistor (VDS) and the current through it (ID) over a transition. We compare this simulated resistance measurement to what we call the “effective resistance.” This effective resistance wouldn’t be the true resistance of the transistor, but rather the apparent resistance as observed from the propagation delay through the transistor.

We use an effective resistance measurement because our overall goal is to calculate delays. With that in mind, the effective resistance must still be close to the true resistance, so that the Elmore delay model is accurate in predicting delays of larger networks of switches.

Figure 6 shows how the effective resistance of an NMOS, taken from the propagation delay, compares to the NMOS’s true resistance . Unfortunately, the two resistances are only comparable in the Super-VT operating range. By using a different average resistance calculation, in which we take the average VDS over the average ID, we actually get close to the effective resistance as far into the Sub-VT range as 0.3 V. This suggests that using this resistance model could work, but it would have limited applicability.

  
**Figure 6. Comparison of Average Resistance   
to Effective Resistance**

# CONCLUSIONS

We have shown in this paper that using a Dual-VDD implementation of a Pass Gate interconnect is better than using either Transmission Gates or Tri-State Inverters in terms of Area, Power, and Delay. We hypothesize that further exploration through analytic modeling and simulations which are more characteristic of FPGA interconnects (by including leaky off switches, etc.) will further support our claim.

# Acknowledgements

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